

What is claimed is:

1        1.        A method of reducing power consumption in a semiconductor memory device having  
2        a row of memory cells and circuitry for operating the row of memory cells, the method  
3        comprising the steps of:

4                providing an intervention circuit;

5                instantiating the intervention circuit within the circuitry for operating the row of  
6        memory cells, proximal to the row of memory cells;

7                operating the intervention circuit to retain the row of memory cells in a desired state;

8        and

9                powering down the circuitry for operating the row of memory cells preceding the  
10       intervention circuit.

1        2.        The method of claim 1, wherein the row of memory cells comprises a wordline and  
2        the circuitry for operating the row of memory cells comprises driver circuitry.

1        3.        The method of claim 1, wherein the intervention circuit comprises a resistor.

1        4.        The method of claim 1, wherein the intervention circuit comprises a transistor.

1        5.        The method of claim 2, wherein the intervention circuit is instantiated such that the  
2        driver circuitry is between the intervention circuit and the wordline.

1       6.       The method of claim 2, wherein the intervention circuit is instantiated between the  
2 wordline and driver circuitry.

1       7.       The method of claim 1, wherein the steps of operating the intervention circuit and  
2 powering down the control circuitry are performed concurrently.

1       8.       The method of claim 7, wherein the intervention circuit is operated by a signal source  
2 that also powers down the control circuitry.

1       9.       The method of claim 1, wherein a nominal delay follows the step of operating the  
2 intervention circuit before powering down the control circuitry is performed.

1       10.      The method of claim 9, wherein the intervention circuit is operated by a first signal  
2 source, separate from a second signal source that powers down the control circuitry.

1       11.      A semiconductor device comprising:  
2               a row of memory cells;  
3               control circuitry preceding the row of memory cells; and  
4               an intervention circuit, instantiated within the control circuitry proximal to the row of  
5 memory cells, adapted to hold the row of memory cells at a desired state while control  
6 circuitry preceding the intervention circuit is powered down.

1       12.     The device of claim 11, wherein the row of memory cells comprises a wordline and  
2     the control circuitry preceding the row of memory cells comprises driver circuitry.

1       13.     The device of claim 11, wherein the intervention circuit comprises a resistor.

1       14.     The device of claim 11, wherein the intervention circuit comprises a transistor.

1       15.     The device of claim 12, wherein the intervention circuit is instantiated such that the  
2     driver circuitry is between the intervention circuit and the wordline.

1       16.     The device of claim 12, wherein the intervention circuit is instantiated between the  
2     wordline and driver circuitry.

1       17.     The device of claim 12, wherein the intervention circuit is coupled to a first assertion  
2     signal source that is also coupled to the driver circuitry.

1       18.     The device of claim 12, wherein the intervention circuit is coupled to a first assertion  
2     signal source, and a second assertion signal source is coupled to the driver circuitry.

1       19.     A wordline circuitry segment in an SRAM device, the circuitry segment comprising:  
2         a first node coupled to a wordline enable signal;  
3         a second node coupled to a wordline signal;  
4         a third node coupled to a sleep mode assertion signal;

5 a fourth node coupled to a first reference voltage;

6 a fifth node coupled to a second reference voltage;

7 a first transistor structure, having a first terminal coupled to the first node, a second  
8 terminal coupled to the fourth node, and a third and fourth terminal;

9 a second transistor structure, having a first terminal coupled to the fourth terminal of  
10 the first transistor structure, a second terminal coupled to the fourth node, a third terminal  
11 coupled to the third terminal of the first transistor structure, and a fourth terminal coupled to  
12 the second node;

13 a third transistor structure, having a first terminal coupled to the third node, a second  
14 terminal coupled to the third terminal of the first transistor structure, and a third terminal  
15 coupled to a third reference voltage; and

16 a fourth transistor structure, having a first terminal coupled to the fifth node, a second  
17 terminal coupled to the fourth node, and a third terminal coupled to the second node.

1 20. The circuitry segment of claim 19, wherein the fifth node is coupled to the third node.

1 21. A wordline circuitry segment in an SRAM device, the circuitry segment comprising:

2 a first node coupled to a wordline enable signal;

3 a second node coupled to a wordline signal;

4 a third node coupled to a sleep mode assertion signal;

5 a fourth node coupled to a first reference voltage;

6 a fifth node coupled to a second reference voltage;

7 a sixth node coupled to a third reference voltage;

8 a first transistor structure, having a first terminal coupled to the first node, a second  
9 terminal, a third terminal coupled to the fifth node, and a fourth terminal;

10 a second transistor structure, having a first terminal coupled to the fourth terminal of  
11 the first transistor structure, a second terminal coupled to the fourth node, a third terminal  
12 coupled to the fifth node, and a fourth terminal coupled to the second node;

13 a third transistor structure, having a first terminal coupled to the third node, a second  
14 terminal coupled to a fourth reference voltage, and a third terminal coupled to the second  
15 terminal of the first transistor structure; and

16 a fourth transistor structure, having a first terminal coupled to the sixth node, a second  
17 terminal coupled to the first terminal of the second transistor structure, and a third terminal  
18 coupled to the fifth node.

1 22. The circuitry segment of claim 21, wherein the sixth node is coupled to the third  
2 node.